REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	10529565	Filing Date	2006-10-31	Docket Number (if applicable)	I431.126.101/FIN481PCT/US	Art Unit	2814
First Named Inventor	Edward Fuergut et al.			Examiner Name	John C. Ingham		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☒ Other Amendment and Response Under 37 C.F.R. 1.116 filed November 2, 2007

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500471

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Mark L. Gleason/	Date (YYYY-MM-DD)	2007-12-27
Name	Mark L. Gleason	Registration Number	39998

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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EXPEDITED PROCEDURE
Examining Group Number 2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Edward Fuergut et al.	Examiner: John C. Ingham
Serial No.:	10/529,565	Group Art Unit: 2814
Filed:	October 31, 2006	Docket No.: I431.126.101/FIN481PCT/US
Title:	ELECTRONIC COMPONENT AND A PANEL	

AMENDMENT AND RESPONSE UNDER 37 C.F.R. 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Amendment and Response is in reply to the Final Office Action mailed August 31, 2007. Please amend the above-identified patent application as follows:

IN THE CLAIMS

Please amend claims 10, 15 and 19 as follows:

1-9. (Cancelled)

10. (Currently Amended) An electronic component comprising:

a stack of semiconductor chips having a first semiconductor chip and a stacked second semiconductor chip, the semiconductor chips having an active first face with contact pads to integrated circuits and a second face;

a flat conductor structure having a chip island, flat conductors surrounding the chip island, and contact pillars arranged on the flat conductors and aligned orthogonally with respect to the flat conductors;

wherein the second semiconductor chip is arranged with its second face on the chip island and wherein its contact pads are electrically connected via bonding wire connections to the flat conductors;

wherein the first semiconductor chip is surrounded by the contact pillars and is arranged underneath the chip island such that pillar contact pads of the contact pillars, first face areas of a plastic encapsulation compound that embeds the semiconductor chips, the contact pillars and the flat conductor structure, and the active first face of the first semiconductor chip, form an overall first face, ~~and~~

wherein a wiring layer is arranged on the overall first face and electrically connects the semiconductor chips to one another via wiring lines, and

wherein the flat conductors extend to edge faces of the plastic encapsulation compound.

11. (Previously Presented) The electronic component of claim 10, wherein the wiring layer comprises a wiring level arranged on the overall first face and comprises outer contact pads that

are electrically connected via the wiring lines to the pillar contact pads of the contact pillars, and/or to the contact pads on the first semiconductor chip.

12. (Previously Presented) The electronic component of claim 10, wherein solder balls are arranged on the outer contact pads.

13. (Previously Presented) The electronic component of claim 10 configured within a panel comprising a leadframe with additional electronic components arranged in rows and columns.

14. (Previously Presented) The electronic component of claim 13, wherein the shape of the panel corresponds in its extent and extent markings to a standard semiconductor wafer.

15. (Currently Amended) A method for production of a panel for a plurality of electronic components comprising:

producing a leadframe with component positions arranged in rows and columns, whereby a component position comprises a chip island and flat conductors which surround the chip island, as well as contact pillars, which are arranged on the flat conductors and are aligned orthogonally with respect to the flat conductors;

applying a stacked semiconductor chip to the chip island of the component positions;

producing bonding wire connections between the flat conductors and contact pads on active first faces of the stacked semiconductor chips;

applying first semiconductor chips with their active first faces to a carrier with adhesive bonding on one side, with the first semiconductor chips being arranged in rows and columns which correspond to the rows and columns of the component positions;

applying the leadframe with stacked semiconductor chips to the carrier in such a way that the contact pillars of the leadframe are adhesively bonded by their first faces to the carrier and the first semiconductor chips are arranged on the carrier underneath the chip islands of the leadframe and are surrounded by contact pillars;

embedding the leadframe with stacked semiconductor chips and bonding wire connections in a plastic compound to form a composite body on the carrier;

removing the carrier exposing an overall first face composed of active first faces of the first semiconductor chips, pillar contact pads of the contact pillars, and an first face of the plastic compound;

applying a wiring layer to the overall first face, forming wiring lines and outer contact pads; and

wherein the wiring lines connect the outer contact pads to the contact pads of the first semiconductor chip, and/or to the pillar contact pads of the contact pillars.

16. (Previously Presented) The method of claim 15 further comprising applying solder balls to the outer contact pads to provide outer contacts.

17. (Previously Presented) The method of claim 15 further comprising separating the panel into individual electronic components.

18. (Previously Presented) The method of claim 17 further comprising applying outer contact pads of an electronic component.

19. (Currently Amended) An electronic component comprising:

a first semiconductor chip having an active first face, contact pads, and a second face;

a stacked second conductor chip having an active first face, contact pads, and a second face;

a chip island;

flat conductors surrounding the chip island;

contact pillars arranged on the flat conductors and surrounding the first semiconductor chip;

wherein the second semiconductor chip is arranged with its second face on the chip island;

means for electrically connecting the contact pads of the second semiconductor chip to the flat connectors;

a plastic encapsulation compound configured to ~~embedd~~ embed the first and second semiconductor chips, the contact pillars, the chip island, and the flat conductors, wherein the flat conductors extend to edge faces of the plastic encapsulation compound;

wherein the first semiconductor chip is arranged under the chip island such that pillar contact pads of the contact pillars, first face areas of the plastic encapsulation compound, and the active first face of the first semiconductor chip form an overall first face; and

means on the overall first face for electrically connecting the first and second semiconductor chips to each other.

20. (Previously Presented) The electronic component of claim 19, wherein the contact pads of the second semiconductor chip are electrically connected to the flat conductors via bonding wire connections.

21. (Previously Presented) The electronic component of claim 19 further comprising a wiring layer arranged on the overall first face and electrically connecting the first and second semiconductor chips to each other via wiring lines.

22. (Previously Presented) The electronic component of claim 21, wherein the wiring layer comprises a wiring level arranged on the overall first face and comprises outer contact pads that are electrically connected via the wiring lines to the pillar contact pads of the contact pillars and to the contact pads on the first semiconductor chip.

23. (Previously Presented) The electronic component of claim 19, wherein solder balls are arranged on the out contact pads.

24. (Previously Presented) The electronic component of claim 19 configured with a panel comprising a leadframe with additional electronic components arranged in rows and columns.

25. (Previously Presented) The electronic component of claim 24, wherein the shaped of the panel corresponds in its extent and extent markings to a standard semiconductor wafer.

REMARKS

The following remarks are made in response to the Final Office Action mailed August 31, 2007. With this Response, claims 10, 15 and 19 have been amended. Claims 10-25 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

Claims 10-25 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hoffman (US 6,737,750) and Ma (US 6,271,469). Applicants respectfully traverse these rejections.

Claims 15-18

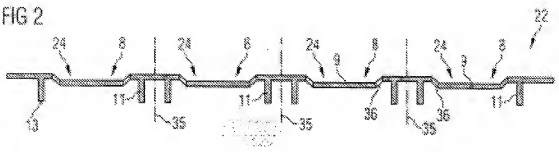
To establish *prima facie* obviousness, the combined prior art references must teach or suggest each claim element. *See* MPEP 2143.03. Applicants respectfully contend that the combination of Hoffman and Ma fail to disclose all claim elements and therefore, the claims are patentable over the combined references.

For example, claim 15 (which has been amended only to correct an informal error) includes

> "producing a leadframe with component positions arranged in rows and columns, whereby a component position comprises a chip island and flat conductors which surround the chip island, …
> applying the leadframe with stacked semiconductor chips to the carrier… [and]
> embedding the leadframe with stacked semiconductor chips and bonding wire connections in a plastic compound to form a composite body on the carrier…."

Figure 2 of the application (reproduced below) illustrates an example of the leadframe 22, including the flat conductor structure 8.

FIG 2



Regarding this element of claim 15, the Office Action refers to col. 12, lines 1-5 of Hoffman, which states,

> "In step 202, a substrate strip for making a plurality of packages 2-1 is provided. The substrate strip includes a single row or a two dimensional array of interconnected substrates 10, which ultimately will be cut apart as a final assembly step."

The Office Action refers to Figure 6A of Hoffman regarding component positions. Figure 6A of Hoffman is reproduced below.

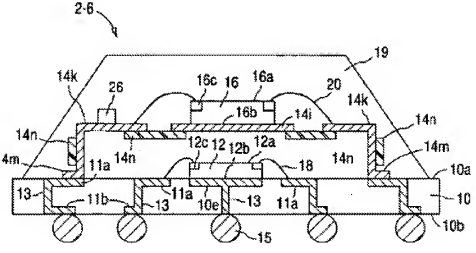


FIG. 6A

Hoffman thus teaches a substrate strip 10 for making packages. However, Hoffman does not disclose a *leadframe* with a plurality of component positions. Rather, a plurality of separate

die pads 14i are attached to the substrate 10. To the extent that the substrate 10 of Hoffman can be considered a "leadframe," Hoffman does not teach encapsulating the "leadframe," or substrate 10. The die pad 14i and leads 14k appear to be encapsulated, but the die pad 14i does not have component positions in rows and columns. Instead, each die pad 14i has a single component position. The substrate 10, which the Office Action equates to the leadframe recited in claim 15, is not encapsulated in the encapsulant 19. Instead, the encapsulant 19 is *over* a portion of the substrate 10, with at least edge portions 10a not covered at all by the encapsulant 10.

In contrast, claim 15 includes providing a leadframe with component positions in rows and columns (see the leadframe 22 and conductor structure 8 in Figure 1 above), and embedding this leadframe with component positions in a plastic compound.

Since the combination of Hoffman and Ma fail to teach or suggest providing a leadframe with component positions in rows and columns, and embedding the leadframe in a plastic compound, this combination of references cannot render claim 15 obvious. Claim 15 is therefore believed to be allowable over the combination of Hoffman and Ma.

Moreover, claims 16-18 all ultimately depend from claim 15 and are therefore allowable for at least the same reasons.

Claims 10-14 and 19-25

Claims 10 and 19 have been amended to more clearly describe the claimed devices. As such, independent claims 10 and 19 each recite, "the flat conductors extend to edge faces of the plastic encapsulation compound."

As noted above, the claimed electronic component is manufactured using a leadframe with a plurality of component positions arranged in rows and columns. Component positions are held together in the leadframe by connections between the flat conductors of adjacent component positions. Therefore, a single leadframe is positioned over a plurality of chips arranged in rows and columns – the lower chips of the stack. After the leadframe is embedded in the plastic

housing and the rewiring layer is applied to the overall upper face to form a panel, the individual packages are singulated from the panel.

Since the upper semiconductor chips are positioned on a leadframe in which the flat conductors of adjacent positions are connected together (see Figure 2 reproduced above), the flat conductors extending between adjacent component positions are severed in the singulation process. Therefore, the metallic edge of the flat conductors extends to the edge faces of the plastic compound. An example of this is illustrated in Figure 1 of the application. In contrast, Hoffman teaches using individual support structures 14 for each component position so that the support structure 14 is positioned entirely within the encapsulation.

Thus, claims 10 and 19 are believed to be allowable over the combination of Hoffman and Ma.

Claims 11-14 and 20-25 all ultimately depend from either claim 10 or 19. As such, they are allowable for at least the same reasons.

CONCLUSION

In view of the above, Applicant respectfully submits that all of the pending claims are in form for allowance. Therefore, entry of this paper is believed proper in accordance with 37 CFR 1.116, and reconsideration and withdrawal of the rejections and allowance of claims are respectfully requested.

No fees are believed to be required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark L. Gleason at Telephone No. (612) 573-2000, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

Edward Fuergut et al.,

By their attorneys,

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